anticipated by Scholz. The Examiner argues that the elements of the invention are anticipated by Scholz.

The Examiner further rejected claims 1-4, 8-10, 14 and 16 under 35 USC 103(a) as being unpatentable over Yasunaga in view of any one of Patents 4,578,214 (Bradley1) and 4,818,823 (Bradley2) to Bradley or Su. The Examiner argues that while Yasunaga uses solder, all three of the references to Bradley and Su teach the use of conductive epoxy. The Examiner argues that the replacement of the solder of Yasunaga with the epoxy of Bradley or Su would be obvious.

The Examiner further argues that Su at column 1, lines 58-63 states that "solder and electrically conductive adhesive are known functional equivalents and are interchangeably used for the same purpose" and cites Smith v. Hayashi, 209 USPQ 754 (Board of Patent Interferences 1980). The Examiner argues that Su in column 1 lines 58-63 and Bradley2 in column 1 lines 25-64 teach that the use of electrically conductive epoxy instead of solder is particularly more attractive because electrically conductive epoxy is a much simpler and less expensive mounting procedure. The Examiner acknowledges that Bradley2 in column 1 lines 34-54 teaches that solder requires the use of high temperatures and the cost involved with an attempt to minimize the shock effects of the high temperatures used in soldering procedures is high.

The Examiner rejected Claim 17 under 35 USC 103(a) as unpatentable over Scholz in view of any one of Lakritz or Japanese references 2-133936 (JREF2) or 1-35528 (JREF1). The Examiner argues that the references taken together as suggested teach the use of spheres as a means for maintaining a minimum bond thickness including at least one sphere.

The Examiner rejected Claim 18 under 35 USC 103(a) as unpatentable over Scholz in view of any one of Lakritz, JREF2, JREF1, or Newman.

The Examiner argues that these references teach the use of spheres as a means for maintaining a minimum bond thickness including at least one sphere. The Examiner argues that Newman further teaches that "because glass spheres have a higher melting temperature than the electrically conductive epoxy, the spheres remain constant during the chip attachment step and therefore the gap between the semiconductor chip and the substrate also remain constant".

The Examiner rejected Claims 17 and 18 under 35 USC 103(a) as being unpatentable over Yasunaga et al in view of any one of Bradley1 or Bradley2, Su as applied to 1-4, 8-10, 14 and 16 above, and further in view of JREF1 and Newman.

The Examiner then reiterates the arguments advanced with respect to Scholz in view of associated references.

Applicant respectfully traverses these rejections.

Rejections Under 35 USC § 102(e)

The Examiner rejected Claims 1-4, 8-10, 14 and 16 over Scholz. In part, the Examiner claims that the "electrically conductive epoxy" of Applicant's invention is shown in Scholz by elements 58 or 60. Elements 58 or 60 of Scholz are contact bumps, and are revealed as being hard enough to allow a press fit due to pressing the bumps into sockets which are fixed in position; see column 5 lines 15-16. The contact bumps are revealed as not being reheated at column 4 line 3 and are formed before assembly of the chip to the substrate.

Applicant uses an epoxy that is liquid when applied, and gently heats the epoxy after assembly of the chip with the substrate, at a lower temperature than solder would require, for the final product. Further, the epoxy of applicant can be repositioned or altered before the final

heating step. Applicant submits that the fixed position preformed contact bumps of Scholz are completely different from the liquid conductive epoxy of Applicant.

Fig. 6 and the specification of Applicant associated with Fig. 6 discloses a chip being in a face up position, which provides a solution to a long felt need for inspecting a mounted flip chip. In prior art attachment methods being compared to the method of Applicant, such as flip-chip technology, inspection of the chip and the bonds after mounting of the chip was not possible. With the invention of Applicant of a method for packaging a flip-chip, that is, not requiring wire bonds, which is capable of being mounted face up, inspection of the chip and of bonds connecting the chip is practical after mounting of the chip. Further, as shown in Fig. 9, backside connection, wherein the chip body is attached to a voltage, is simplified and improved.

In the prior art, the backside was generally connected on the face of the chip, requiring extra surface space and a special connection, and resulting in an additional resistance being introduced in the connection. With Fig. 9, connection directly to the backside is made when the flip-chip is face up, which is especially advantageous with, for example, power circuits. Where a low resistance to the backside is desired, Applicant provides a solution that was previously available only without flip chip mounting. A method such as disclosed by Applicant for connecting the front side circuitry of a chip while simultaneously making a large area, low resistance connection to the backside without requiring wire bonds is very desirable. Low resistance backside contacting was difficult or impossible for flip-chips until the present invention of a flip chip packaging apparatus and method capable of providing face up mounting.

Applicant respectfully submits that the connection of a flip chip to a board with the chip face up, that is, with chip connections to the board from the side of the chip farthest from the

board, is novel and non-obvious. Further, spraying or inking the epoxy on a flip-chip in a face up position for connecting the flip-chip to a substrate is not revealed in any of the refereneces. Scholz does not disclose or suggest a flip chip connected to a board or substrate face up with the bonds and the circuitry on the chip capable of being inspected on the completed assembly.

Rejections Under 35 USC § 103(a)

The Examiner rejected Claims 1-4, 8-10, 14 and 16 Yasunaga in view of Bradley 1, Bradley 2 or Su. The Examiner further comments that all the references "establish that, before the invention by the applicant, those in the art recognized the functional interchangeability of between solder and electrically conductive epoxy". The Examiner then cites Su and Bradley2, including a quote from Bradley2 at column 1 lines 34-54 that "solder requires the use of high temperatures and the cost involved with an attempt to minimize the shock effects of the high temperatures used in soldering procedures is high." Since solder creates shock effects when compared to conductive epoxy, it is submitted that solder and conductive epoxy are not functionally equivalent.

Applicant submits that conductive epoxy is applied as a liquid at room temperature, and can be painted on, inked on, or applied in ways conducive to easily making, for example, repairs and alterations. Further, the epoxy can be applied such that the face up surface of a chip may be connected to the substrate without additional wiring or external components. Applicant reveals mounting a chip face up, then patterning a conductive epoxy from the face of the chip, down the beveled sides, to the substrate, for making a sprayed on or inked on connection across the

thickness of the chip. This desirable result is not revealed in any of the cited references. Applicant specifically further submits that this result cannot be achieved using solder.

Solder is not liquid until it is heated to temperatures that do not allow it to be easily painted or inked onto a substrate or other media for establishing a connection. Applicant submits that solder and conductive epoxy are not functional equivalents for all purposes, though they may share common properties such as adhesion and conductivity. For the purpose of this invention, they are not equivalent; applicant uses a chip in which conductive epoxy may be used to minimize the shock of heating. Post assembly heating of the conductive epoxy is at a lower temperature than is required for solder and does not involve soldering shock effects.

The Examiner rejected claim 17 over Scholz in view of any one of Lakritz, JREF2 or JREF1. The Examiner argues that these references teach using spheres, including glass spheres, for maintaining a desired thickness or spacing between external connections of a semiconductor chip and the terminals on a substrate. Applicant respectfully traverses this rejection.

Scholz teaches a deformable bump at column 4 lines 35-40, which is permanently affixed to either or both the chip and the substrate. The permanent bumps of Scholz cannot be compared to loose spheres immersed in an adhesive such as conductive epoxy as with the present invention. Also, Scholz uses his bumps for connection, not spacing, and teaches forcing the spheres into a socket or similar connection, stressing the assembly. Scholz teaches that his layer 70 be a compliant material that allows some deformation, such as at column 5 lines 67-68, a limitation not found in the invention. In any case, Scholz does not teach using spheres, and does not teach his bumps included in a liquid and free to move.

Lakritz teaches conductive spacers which are columns and are in fixed, predefined locations, and are never loose or free to move. Applicant submits that the spheres of Applicant are immersed in the epoxy, and are free to move as the epoxy is worked prior to curing the epoxy. Further; the spheres of the invention are not conductive, and are used only as spacers, not conductors as in Lakritz. Additionally, Lakritz teaches an hour-glass shaped solder terminal at column 2 lines 11-14. It is well known, as acknowledged in several of the cited references, that an hour-glass shaped conductive epoxy terminal would not be superior for withstanding stress. This is shown in Newman in his figures 3a and 3b and the accompanying descriptions, where it is revealed that even at very small spacing (substantially less than .006 inches (6 mils) is shown, and preferably 2-4 mils is indicated) stress is induced. The hour-glass shaped attachment of Lakritz, which is revealed to be 5 mils nominal, requires that the column be large enough and strong enough to bridge the 5 mil gap with surface tension effects. Relatively large, thick columns of solder will create stress due to surface tension. These stresses are not present with the small spacing and low forces disclosed by Applicant.

It is submitted that the Japanese references both teach away from the invention. JREF1 teaches spacers for use in a display terminal. Spacing the gap between the outer layers of a display is entirely different than spacing a chip from a board. Applicant respectfully submits that both the adhesive layers 7 and 8 are revealed as abutting and being conductive. Since the two layers are revealed as abutting and conductive, there is a short circuit everywhere, with no separate, clearly defined terminal areas as in the invention.

JREF2 teaches a conductive particle for enhancing the connectivity while providing a spacer. It is not obvious to substitute a non-conductive glass spacer of the invention in light of

the teaching of a conductive spacer of this reference; rather, the reference teaches away from the invention by teaching a conductive sphere in the conductive areas. In this reference, the spacers are revealed as being both small conductive spheres in the conductive areas and larger nonconductive spheres in the nonconductive areas. The fourth line from the bottom of this reference states that an adhesive containing a conductive particle is applied at the terminals. A gap material, shown in the attached figure as including spheres immersed in an adhesive, is located "where the conductive particle does not exist", indicating that the spheres in the gap material are not conductive. It is clear that the reference does not teach providing both spacing and conduction at a point, with nonconductive glass spheres located in the conductive areas as is true in the invention. In this sense, by teaching conductive particles in the conductive areas, and nonconductive particles in the nonconductive areas, the reference teaches away from the invention.

Newman teaches silver filled glass spheres, which, as Newman teaches at column 3 lines 46-48, are conductive. Newman also teaches the spheres are heated to the point of collapse, providing a smaller sphere for filling voids. In this regard, Newman teaches a high temperature process using conductive particles reformable to a smaller size during assembly, and teaches away from the invention. Applicant teaches a low temperature process using nonconductive spheres that do not change size, a completely different approach to the problem of providing both conduction and spacing. Conductive glass spheres containing, e.g., silver, cannot be compared to nonconductive glass spheres used for spacing in a contact area only. Applicant submits that high temperature collapsible spheres used for occluding voids cannot be compared to low temperature

spheres which do not collapse or change size. By teaching the use of high temperature collapsing glass spheres Newman teaches away from the invention.

The Examiner rejected Claims 17 and 18 over Yasunaga in view of Bradley 1, Bradley 2, Su, JREF1 or Newman. The Examiner argues that Yasunaga in view of JREF1 and Newman teach all the elements of the invention.

Applicant respectfully submits that Yasunaga teaches a bump affixed at a predefined location, not a glass sphere mixed in an adhesive as in the invention. All three of the references teach conductive spacers. The resizable glass sphere of Newman having silver admixed to provide a conductive spacer is very different from the fixed size nonconductive glass spheres of Applicant. Conductors and nonconductors are respectfully submitted to be separate functional elements, even when the basic material is the same.

The Examiner further states that Newman in column 5 lines 53-62 teaches that because "glass spheres have a higher melting temperature than the electrically conductive epoxy, the spheres remain constant during the chip attachment step and the gap between the semiconductor chip and the substrate also remain constant." Applicant respectfully traverses this argument. The quotation cited relates to a quality which Newman teaches is a deficiency creating a problem to be solved. As shown at column 5 lines 61 and 62, Newman teaches that the above procedure causes voids which undesirably decrease shear strength and conductivity. At column 6 lines 4 – 15 Newman teaches solving the problem of voids by providing deformable spheres 14 and 20 that decrease the size of the spacers 20 to conform to the decrease in size of the spacers 14. Applicant respectfully submits that the citation also teaches away from the invention by teaching

at column 5 lines 61-62 that maintaining a constant gap between the semiconductor chip and the substrate is undesirable.

All the references cited teach conductive spacers in the conductive areas. Applicant respectfully submits that all the references teach away from the invention, which discloses nonconductive glass spheres in the conductive areas.

To support the position that solder and electrically conductive adhesive are known functional equivalents and are interchangeably used for the same purpose, the Examiner directed Applicant's attention to Bradley1, Bradley2 and Su, all of which are relied on by the Examiner in the above rejection.

Applicant traverses this contention. Solder and electrically conductive adhesive share common properties relating to conduction and adhesion in an appropriately limited sense. However, solder and electrically conductive epoxy are not functional equivalents and are not interchangeably used for all purposes. Bradley 1, for example, at column 8 lines 8 – 9 states "This material will generally be supplied in fluid or paste form, with or without an evaporating solvent" whereby it is clear that a room temperature liquid application is taught. Solder is not liquid at room temperature, and Applicant submits it cannot be supplied in fluid or paste form at room temperature as taught. Bradley 1 goes on to specify room temperature "application by spray, brush, dip, or other suitable method". Solder cannot be used to spray, brush or dip at room temperature. Applicant also submits that solder requires a corrosive flux for providing an adherent surface. Conductive epoxy does not require a flux, which further distinguishes conductive epoxy from solder.

Bradley 2, at column 1 lines 59-64 discloses that high temperatures are necessary for soldering operations. Bradley 2 states "Instead of using heat to effect the connection, this invention uses a pressure sensitive adhesive and an electrically conductive medium to mechanically and electrically attach the component in place removing the expense and component rejection associated with methods utilizing a high heat device." Applicant submits that by distinguishing between solder and conductive epoxy, Bradley 2 teaches that for the intended purpose of his patent, and therefore for this invention where only low heating is employed, solder and conductive epoxy are not interchangeable and not functionally equivalent.

Su teaches, at column 1 lines 58 – 63, that "Conductive adhesives have certain unique properties that make them particularly attractive for use in attaching components to printed circuit boards. One advantage is that these adhesives provide a much simpler assembly procedure, than do wave solder or reflow solder processes." Applicant submits since conductive adhesives such as the conductive epoxy of Applicant have are taught to have "certain unique properties" compared to solder, solder and conductive epoxies are not functionally equivalent, even though they share a limited range of properties.

All of the cited references of the Examiner that discuss both solder and epoxy distinguish between them. As shown in the cited references, and for the purposes of this invention, solder and conductive epoxy are not functionally equivalent.

In view of the foregoing, it is believed that Claims 1-18 pending herein are now in condition for allowance. Applicant respectfully urges the Examiner to withdraw his objections and rejections hereto and allow the application to advance to allowance.

Respectfully submitted,

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